DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 320240C FGH-PW (A-TOUCH)

Product specification ***Version: 4***

14/Sep/2011

GENERAL SPECIFICATION

MODULE NO. :

DEM 320240C FGH-PW (A-TOUCH)

CUSTOMER P/N

VERSION NO.	CHANGE DESCRIPTION	DATE
0	Original Version	09.07.2007
1	Add Jumper Setting and Power Supply Description	19.07.2007
2	Update Specification	07.05.2008
3	Change PCB Description	20.10.2008
4	Adding Version	14.09.2011

PREPARED BY: LX DATE: 14.09.2011

APPROVED BY: MHO DATE: 14.09.2011

CONTENTS

1. FUNCTIONS &FEATURES

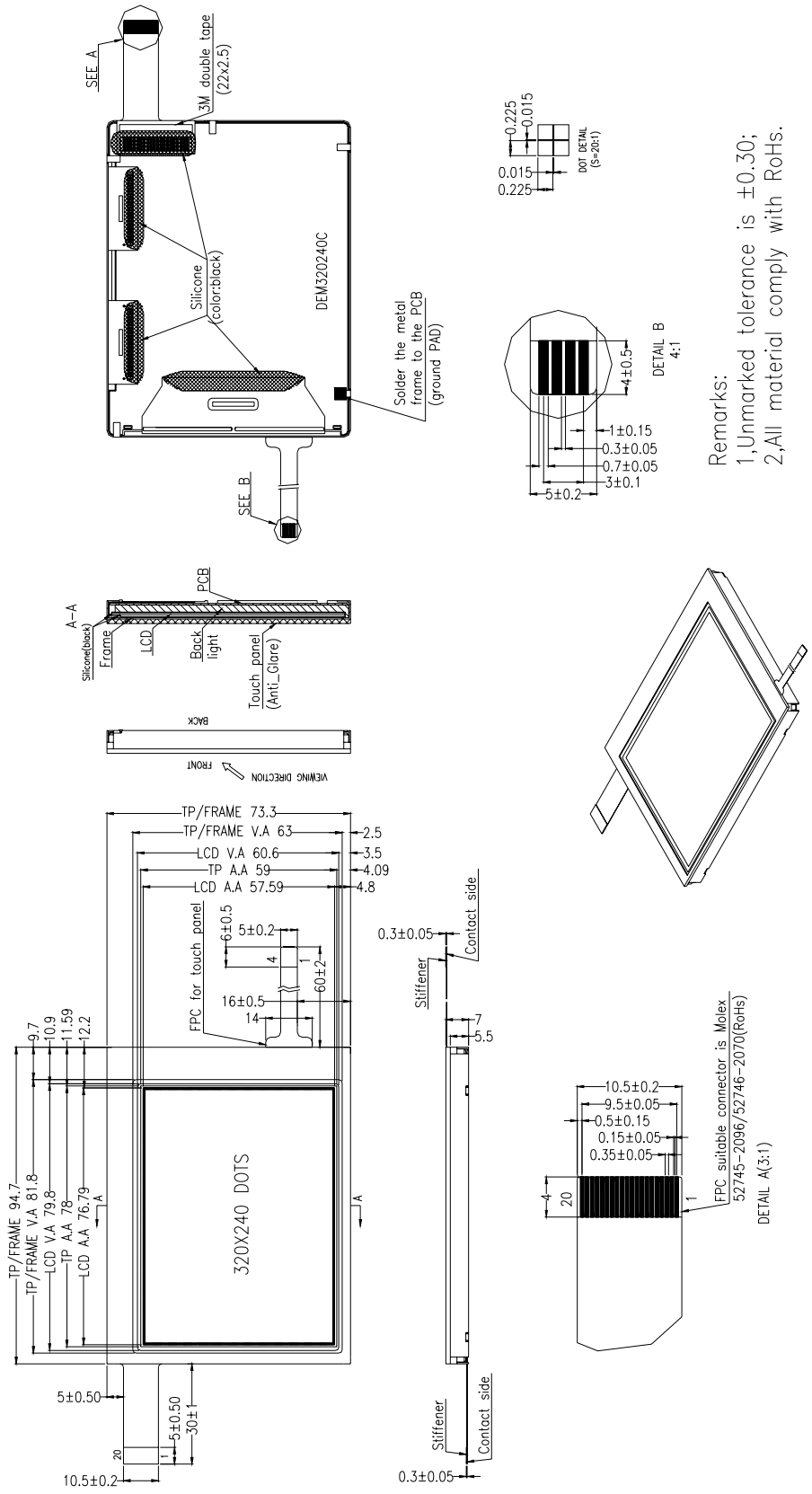
MODULE NAME	LCD TYPE
DEM 320240C FGH-PW (A-TOUCH)	FSTN Transflective Positive Mode

- Display Format : 320 x 240 Dots, ¼ VGA
- Viewing Direction : 6 O'clock
- Driving Scheme : 1/240 Duty, 1/13 Bias,
- Supply voltage : 5Volt (typ.)
- V_{LCD} : 22.5Volt (typ.)
- Backlight color : LED, Lightguide, White
- Interface : Parallel
- Control IC : S1D13700 (Epson)
- Operating Temperature : -20°C to +70°C
- Storage Temperature : -30°C to +80°C
- Touch Panel : 4-Wire-Resistive-Analog Touch-Panel on Board
- RoHS : Compliant

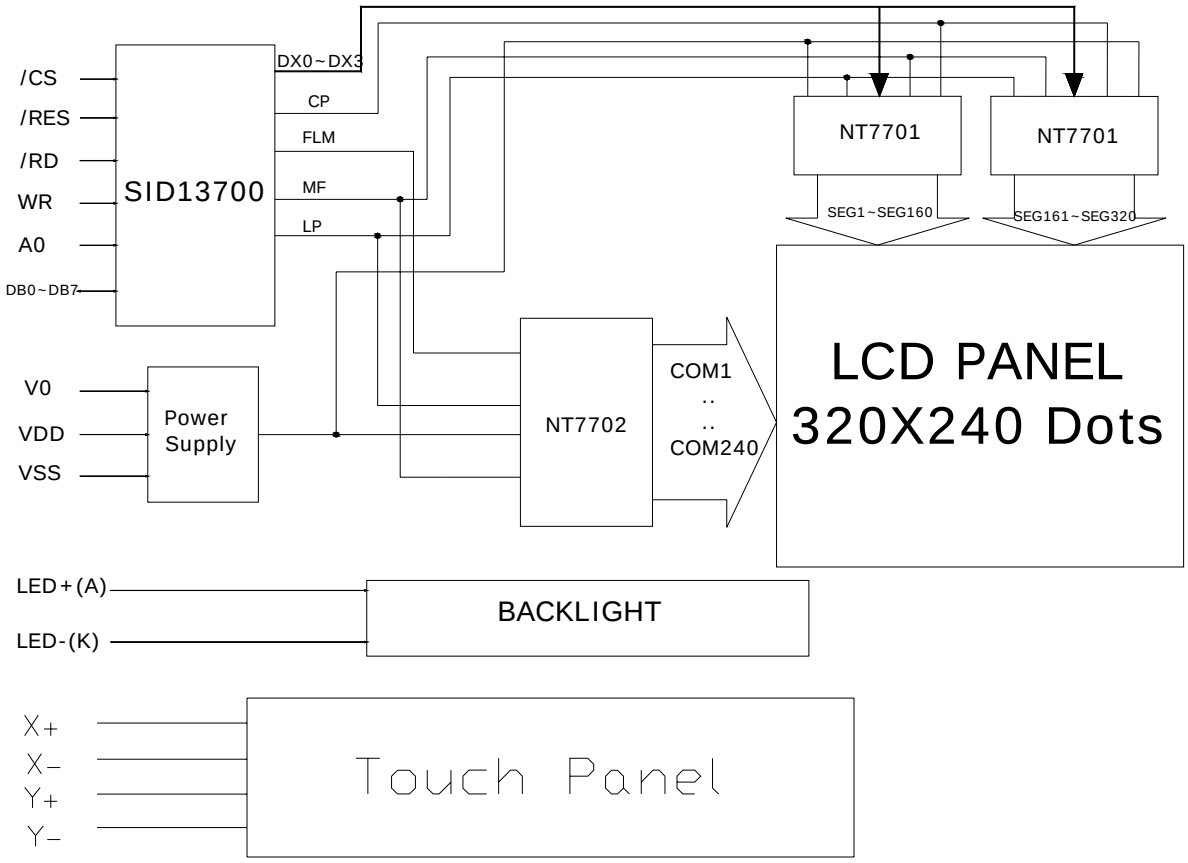
2. MODULE ARTWORK

- Module size : 94.70 mm x 73.30 mm x 7.00 mm
- Metal frame Viewing Area : 81.80 mm x 63.00 mm
- LCD Viewing Area : 79.80 mm x 60.60 mm
- Dot Pitch : : 0.24 mm x 0.24 mm
- Dot Size : 0.225 mm x 0.225 mm
- Dot Gap : 0.015 mm

3. EXTERNAL DIMENSIONS



4. BLOCK DIAGRAM



5.PIN ASSIGNMENT

5.1 MODULE PIN ASSIGNMENT

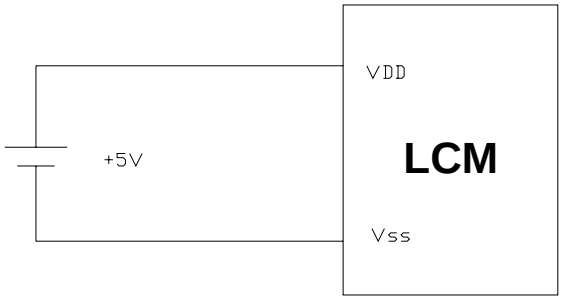
Pin No.	Symbol	Function
1	V_{SS}	Ground terminal of module
2	V_{DD}	Power terminal of module 2.7V to 5.5V (TYP: 5V)
3	V_0	Contrast voltage for LCD drive (variable)
4	V_{OUT}	Voltage booster output terminal.
5	/WR	8080family: Write signal; 6800 family: R/W signal
6	/RD	8080 family: Read signal; 6800 family: Enable clock (E)
7	/CS	Chip select. This active-low input enables the S1D13700. It is usually connected to the output of an address decoder device that maps the S1D13700 into the memory space of the controlling microprocessor
8	A0	System Address select. For Direct addressing mode, this pin is used for system address bit 0. For Indirect addressing mode, this pin in conjunction with RD# and WR# determines the type of data present on the data bus
9	/RES	Reset signal
10~17	DB0~DB7	Data bus
18	NC	No used
19	LED+(A)	Anode for backlight
20	LED-(K)	Cathode for backlight

5.2 TOUCH PANEL PIN ASSIGNMENT

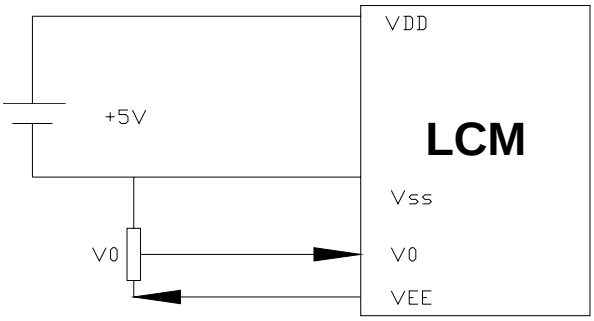
Pin No.	Symbol	Function
1	Y-	Y- Position Input
2	X+	X+ Position Input
3	Y+	Y+ Position Input
4	X-	X- Position Input

6. POWER SUPPLY

Mode(Internal contrast regulation)-J7 is close



Mode(external contrast regulation)-J7 is open



7. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply voltage Logic	VDD	-0.3	7.0	V
Input voltage	--	-0.3	VDD+0.3	V
Supply voltage Vo	Vlcd	-0.3	30	
Operating Temperature	---	-20	+70	ºC
Storage temperature	--	-30	+80	ºC

8. BACKLIGHT ELECTRICAL/OPTICAL SPECIFICATIONS

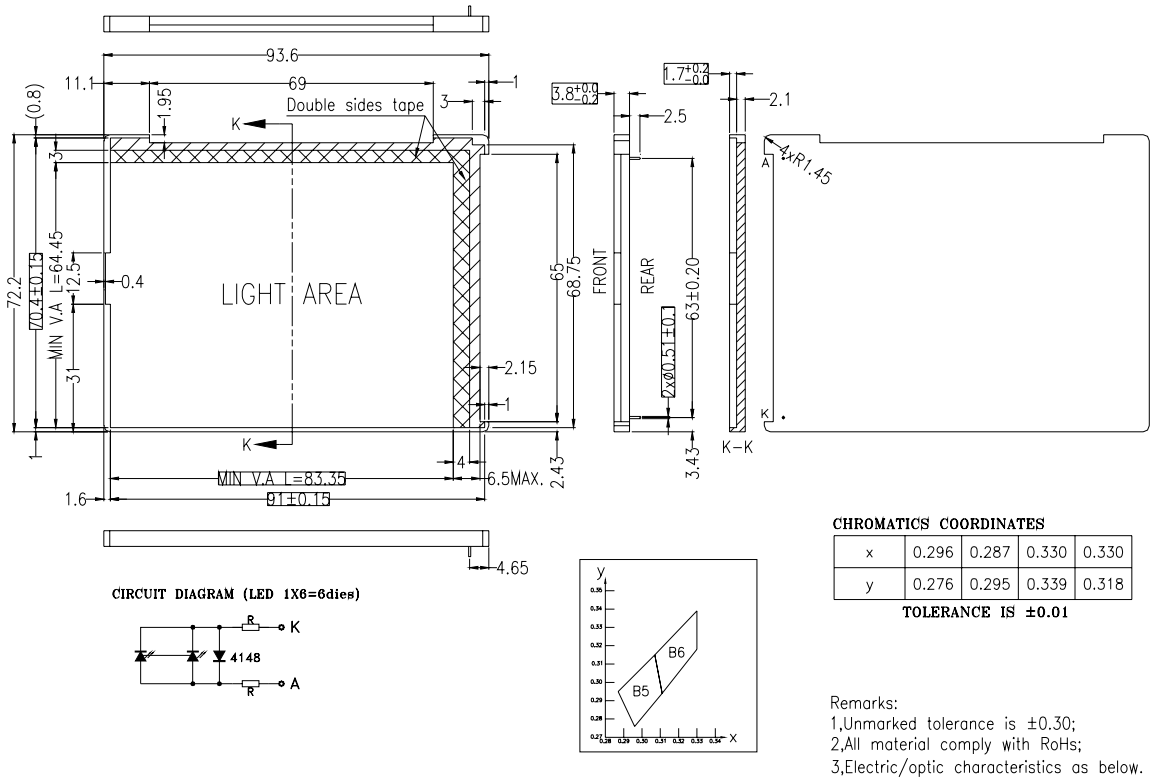
Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Conditions	Rating	Unit
Absolute Maximum Forward Current	Ifm		150	mA
Peak Forward Current	Ifp	1 Msec Plus 10% Duty Cycle	360	mA
Reverse Voltage	Vr		1	V
Power Dissipation	Pd		450	mW
Lifetime		If=90mA	30 000	h

Backlight Electro/Optical Characteristics

Item	Symbol	min.	typ.	max.	Unit	Condition
Forward Voltage	Vf	3.7	4.0	4.3	V	If= 90 mA
Reverse Current	Ir			50	μA	Vr= 0.8 V
Peak wave length	λp		White		nm	If= 90 mA
Spectral Line Half width	Δλ				nm	If= 90 mA
Luminance	Lv	210	400		cd/m²	If= 90 mA

Backlight Drawing



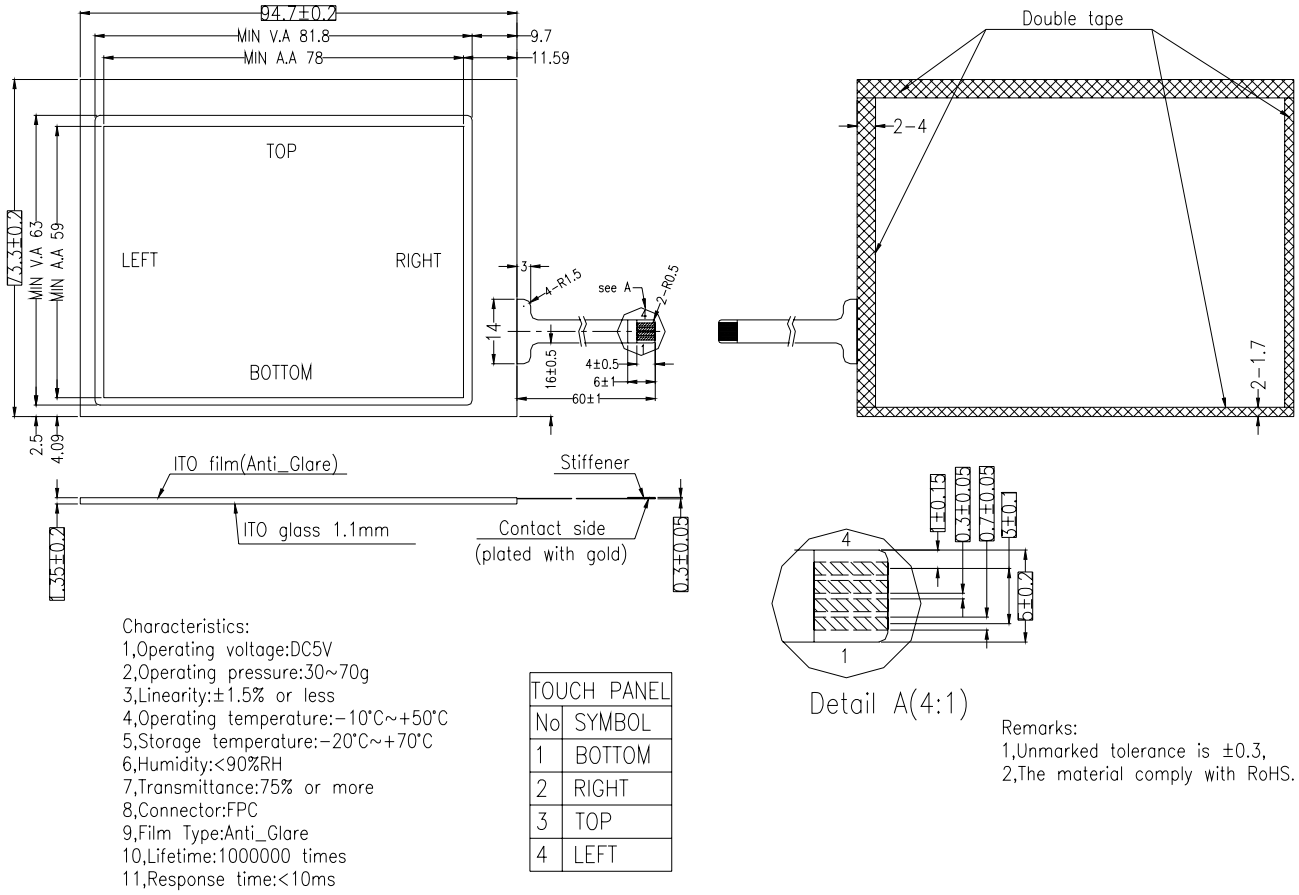
CHROMATICS COORDINATES

x	0.296	0.287	0.330	0.330
y	0.276	0.295	0.339	0.318

TOLERANCE IS ±0.01

Remarks:
1,Unmarked tolerance is ±0.30;
2,All material comply with RoHs;
3,Electric/optic characteristics as below.

9. TOUCH PANEL

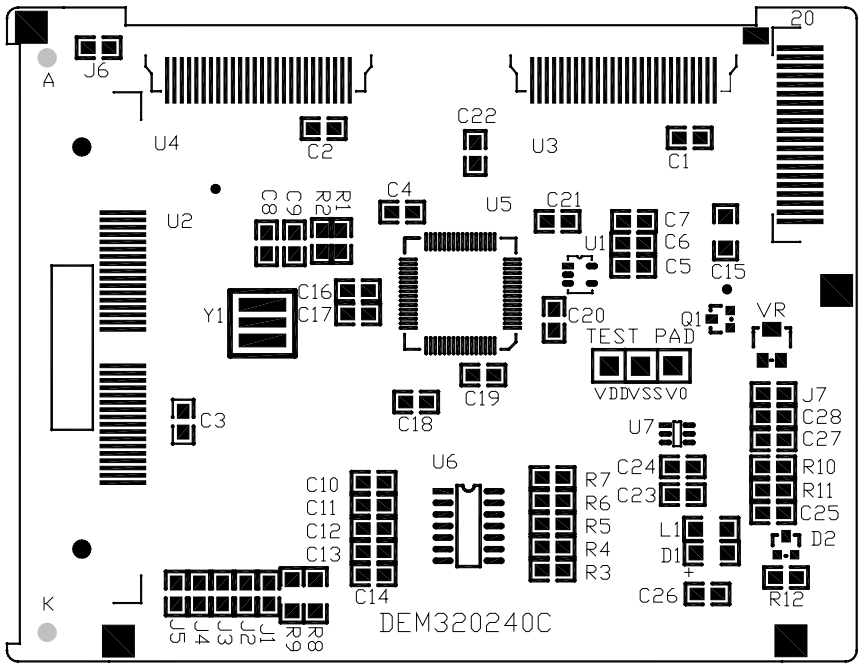


Characteristics:
1,Operating voltage:DC5V
2,Operating pressure:30~70g
3,Linearity:±1.5% or less
4,Operating temperature:−10°C~+50°C
5,Storage temperature:−20°C~+70°C
6,Humidity:<90%RH
7,Transmittance:75% or more
8,Connector:FPC
9,Film Type:Anti_Glare
10,Lifetime:1000000 times
11,Response time:<10ms

TOUCH PANEL	
No	SYMBOL
1	BOTTOM
2	RIGHT
3	TOP
4	LEFT

Remarks:
1,Unmarked tolerance is ±0.3,
2,The material comply with RoHS.

10. PCB DRAWING AND DESCRIPTION



10.1 DESCRIPTION

10-1-1.The polarity of the pin 19 and the pin 20:

J3,J5	J2, J4	LED Polarity	
		19Pin	20Pin
Each open	Each closed	Anode	Cathode
Each closed	Each open	Cathode	Anode

Note: In application module, J3=J5 = openJ2=J4=0 ohm.

10-1-2. The metal frame contacts need to be on GND if J6 is closed..

Note: In application module, J6= Open,

10-1-3.The LED resistor should be bridged when J1 is closed

Note: In application module, J1=open

10-1-4.The R8 and R9 are the LED resistor.

Note: In application module, R8=10 Ohm, R9=open

10-1-5. If module use internal voltage supply V0, the J7 should be closed

If module use external Voltage supply V0, the J7 should be open

Note: In application module, J7=open.(First, J7=close, must adjust LCD to best contrast before shipment)

10-1-6. The VR10 is variable resistor for regulating LCD driving voltage V0.

In application module, VR=10K ohm.

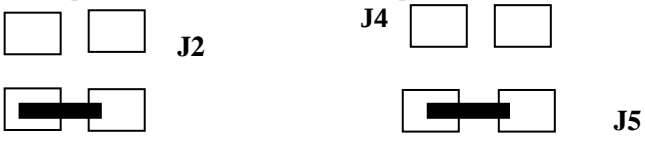
10.2 Example application

10-2-1. The LED resistor should be bridged as following.

R8

10-2-2. The 19 pin is the anode and the 20 pin is the cathode as following.

10-2-3.The 19 pin is the cathode and the 20 pin is the anode as following.



11. DC CHARACTERISTICS

(V_{SS}= 0V, Ta = -20 to +70ºC)

Parameter	Symbol	Min.	Typ	Max	Unit
Supply Voltage Logic	V_{DD}	4.7	5	5.3	V
Consumed current	I_i	---	TBD	---	mA
LCD driving voltage	--	15	22.5	30	V

12. AC CHARACTERISTICS

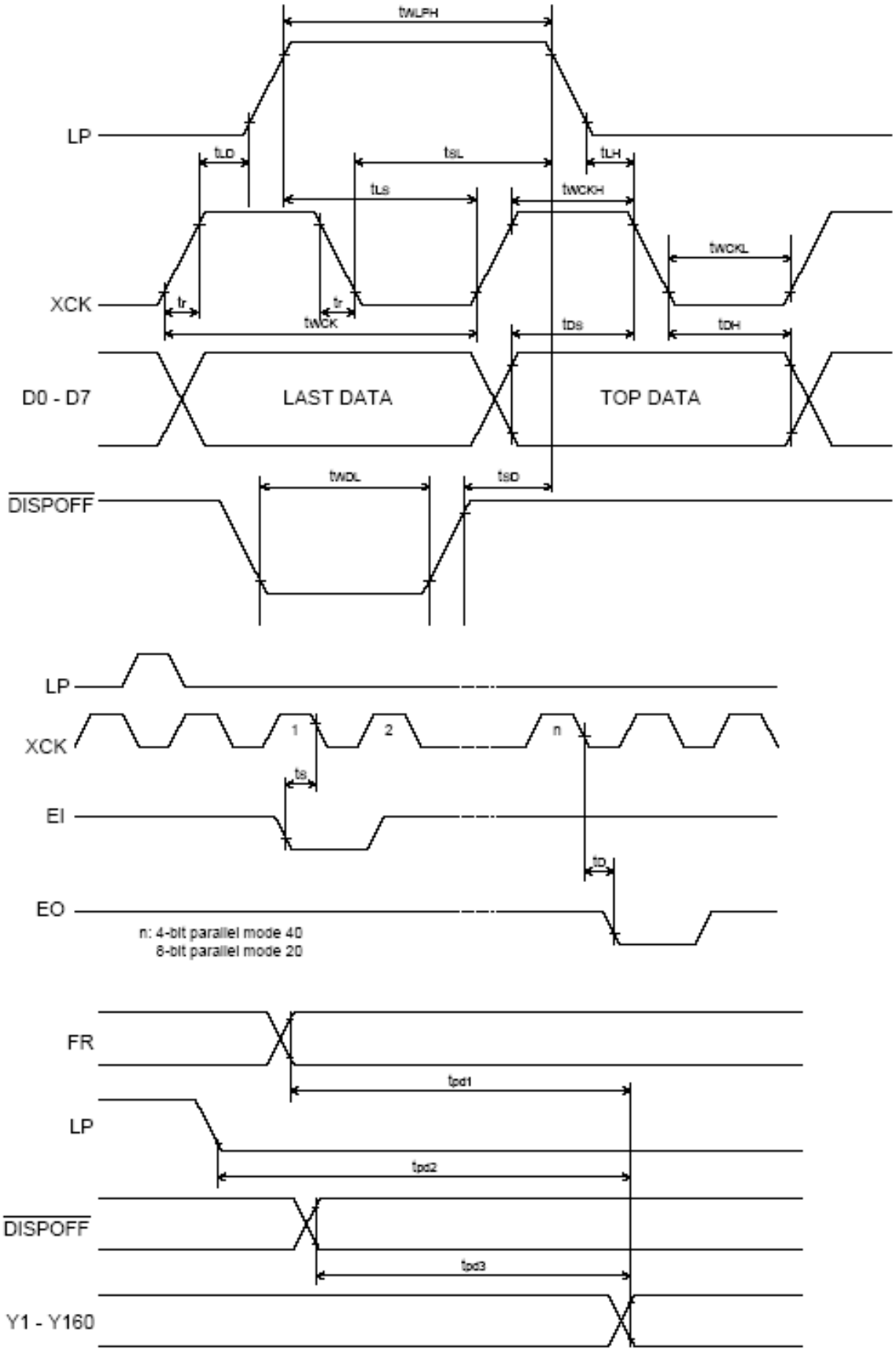
12.1. NT7701 Segment Mode AC Characteristics

(V_{SS}= 0V, Ta=-20~+70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	125	-		ns	tr, tf ≦ 11ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	51	-		ns	
Shift clock "L" pulse width	t_{WCKL}	51	-		ns	
Data setup time	t_{DS}	30	-		ns	
Data hole time	t_{DH}	40	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	51	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	51	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	51	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	51	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	36	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	78	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL = 15pF

Note

1. Take the cascade connection into consideration.
2. (t_{CK} - t_{WCKII} - t_{WCKL})/2 is the maximum in the case of high speed operation.

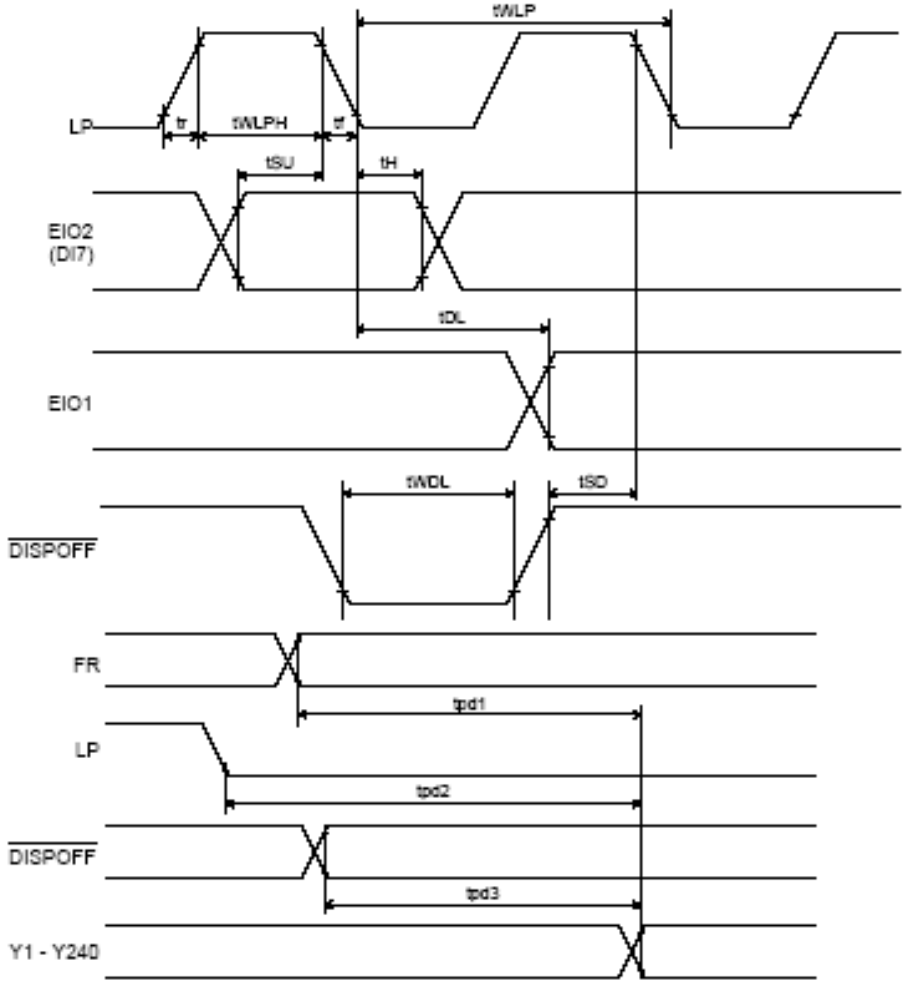


Timing Characteristics of segment Mode

12.2 NT7702 Common Mode AC Characteristics

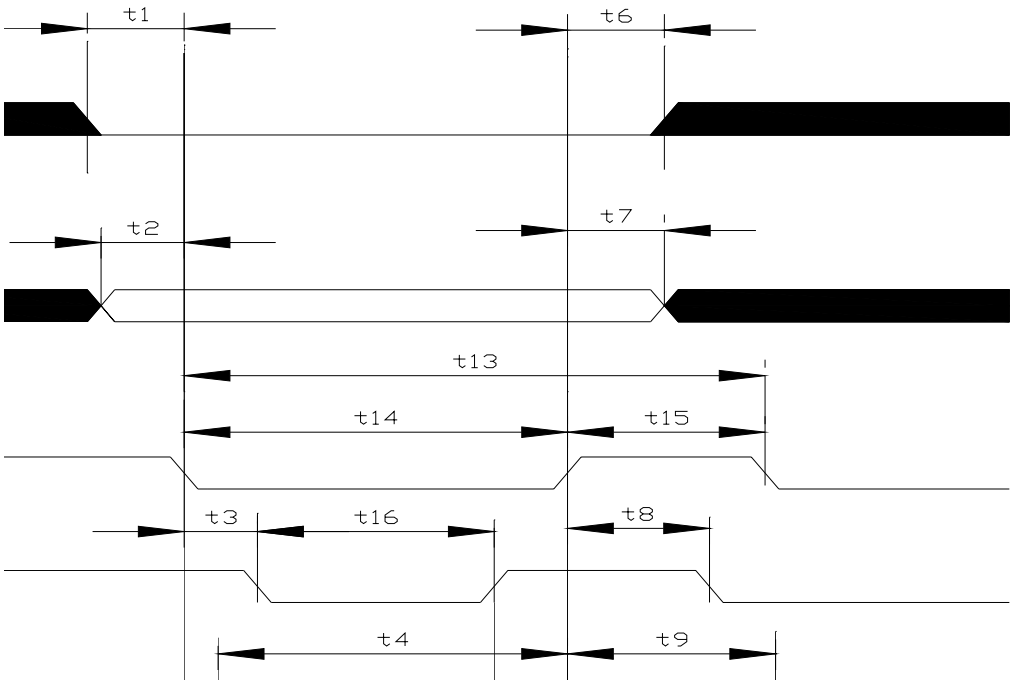
(V_{SS} =0V, Ta=-20~70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WLP}	250	-	-	ns	tr, tr ≦ 20ns
Shift clock "H" pulse width	t_{WLPH}	15	-	-	ns	V_{DD} = +5.0V ± 10%
		30	-	-	ns	V_{DD} = +2.5 - +4.5V
Data setup time	t_{SU}	30	-	-	ns	
Data hole time	t_H	50	-	-	ns	
Input signal rise time	tr		-	50	ns	
Input signal fall time	tr		-	50	ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-	-	ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-	-	µs	
Output delay time (1)	t_{DL}	-	-	200	ns	C_L = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}	-	-	1.2	µs	C_L = 15pF
Output delay time (3)	t_{pd3}	-	-	1.2	µs	C_L = 15pF



13. S1D13700 TIMING DIAGRAMS

Generic Bus Direct/Indirect Interface with WAIT Timing



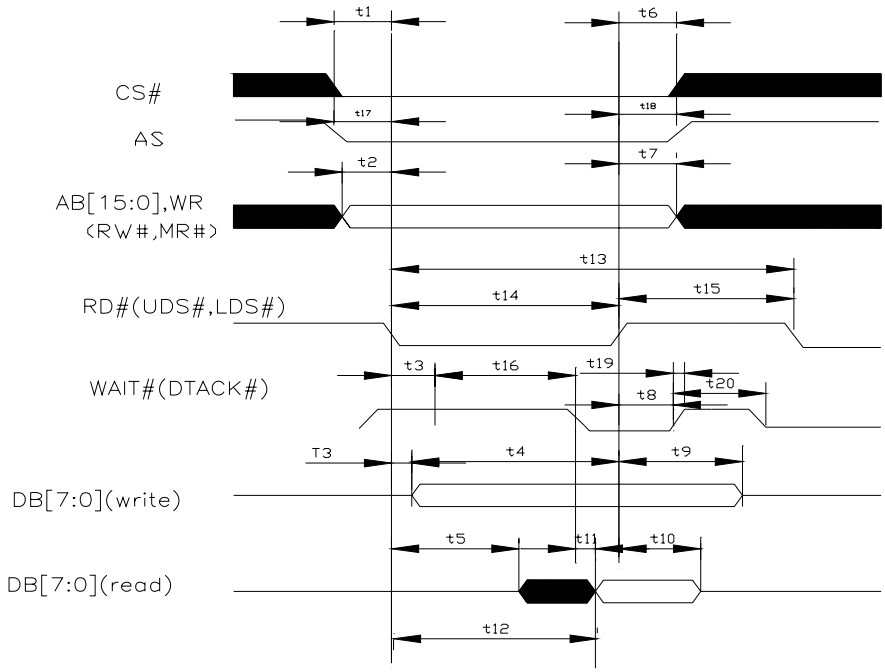
Generic Bus Direct/Indirect Interface with WAIT Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	--	5	--	ns
t2	AB[15:0] setup time	5	--	5	--	ns
t3	WR#, RD# falling edge to WAIT# driven low	2	15	2	--	ns
t4	DB[7:0] setup time to WR# rising edge (write cycle)	Note2	--	Note2	15	ns
t5	RD# falling edge to DB[7:0] driven (read cycle)	3	--	3	--	ns
t6	CS# hold time	7	--	7	--	ns
t7	AB[15:0] hold time	7	--	7	--	ns
t8	RD#, WR# rising edge to WAIT# high impedance	2	10	2	10	ns
t9	DB[7:0] hold time from WR# rising edge (write cycle)	5	--	5	--	ns
t10	DB[7:0] hold time from RD# rising edge (read cycle)	3	14	3	14	ns
t11	WAIT# rising edge to valid Data if WAIT# is used	--	Note3	--	Note 3	ns
t12	RD# falling edge to valid Data if WAIT# is not used	--	Note 4	--	Note 4	ns
t13	RD#, WR# cycle time	Note5	--	Note5	--	ns
t14	RD#, WR# pulse active time	5	--	5	--	Ts
t15	RD#, WR# pulse inactive time	Note6	--	Note 6	--	ns
t16	WAIT# pulse active time	--	Note7	--	Note 7	ns

Note:

1. Ts = System clock period
2. t4min = 2Ts + 5
3. t11max = 1Ts + 5 (for 3.3V)
   = 1Ts + 7 (for 5.0V)
4. t12max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
5. t13min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
6. t15min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)
7. t16max = 4Ts + 2

C68K Family Bus Indirect/Direct Interface with DTACK# Timing

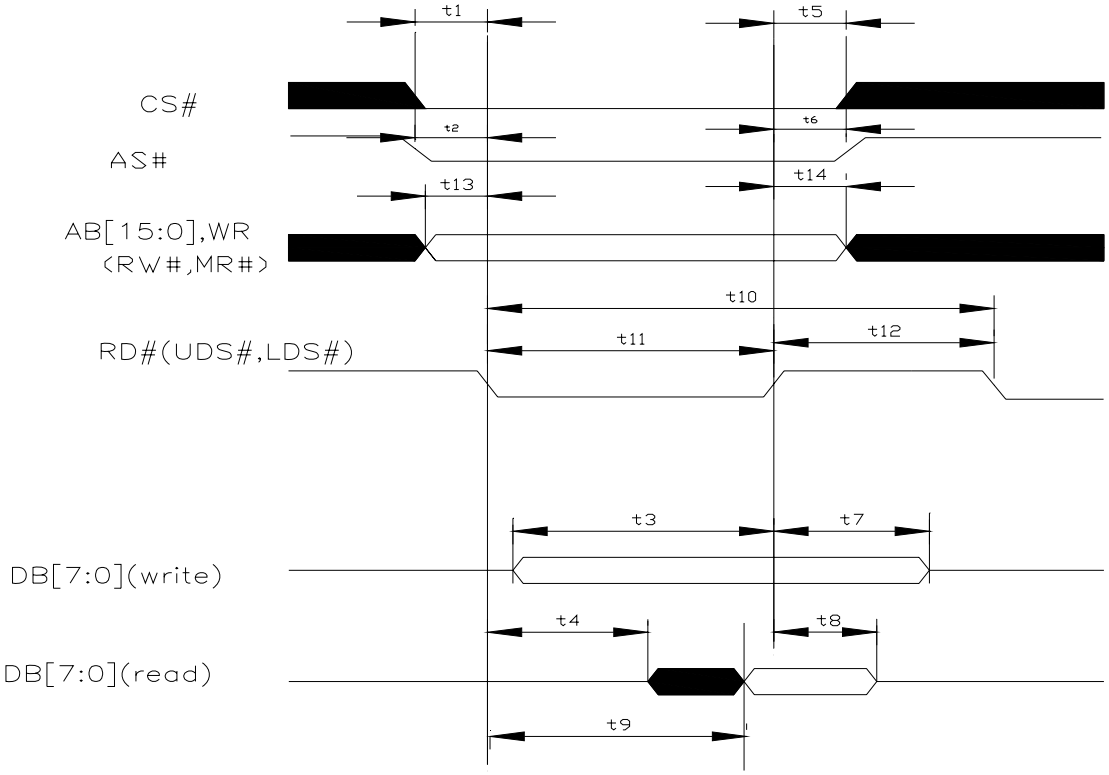


Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	--	5	--	ns
t2	AB[15:0] setup time	5	--	5	--	ns
t3	AS# falling edge to WAIT# driven	2	15	2	15	ns
t4	DB[7:0] setup time to RD# rising edge (write cycle)	Note2	--	Note2	--	ns
t5	RD# falling edge to DB[7:0] driven (read cycle)	3	--	3	--	ns
t6	CS# hold time	7	--	7	--	ns
t7	AB[15:0] hold time	7	--	7	--	ns
t8	RD# rising edge to WAIT# high impedance if Direct interface and in Power Save Mode	2	10	2	10	ns
t9	DB[7:0] hold time from RD# rising edge (write cycle)	5	--	5	--	ns
t10	DB[7:0] hold time from RD# rising edge (read cycle)	2	55	2	55	ns
t11	WAIT# falling edge to valid Data if WAIT# is used	--	Note3	--	Note 3	ns
t12	RD# falling edge to valid Data if WAIT# is not used	--	Note 4	--	Note 4	ns
t13	RD# cycle time	Note5	--	Note5	--	ns
t14	RD# pulse active time	5	--	5	--	Ts
t15	RD# pulse inactive time	Note6	--	Note 6	--	ns
t16	WAIT# pulse inactive time from WAIT# driven	--	Note7	--	Note 7	Ns
17	AS# setup time	0	--	0	--	ns
18	AS# hold time	0	--	0	--	ns
19	AS# rising edge to WAIT# high de-asserted if not Direct interface and not in Power Save Mode	--	10	--	10	ns
20	WAIT# pulse inactive time	0	Note 8	0	Note 8	ns

Note:

1. Ts = System clock period
2. t4min = 2Ts + 5
3. t11max = 1Ts + 5 (for 3.3V)
   = 1Ts + 7 (for 5.0V)
4. t12max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
5. t13min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
6. t15min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)
7. t16max = 4Ts + 2
8. t20max = 1Ts - 15

MC68K Family Bus Indirect/Direct Interface without DTACK# Timing



Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	--	5	--	ns
t2	AB[15:0] setup time	5	--	5	--	ns
t3	DB[7:0] setup time to RD# rising edge (write cycle)	Note2	--	Note2	--	ns
t4	RD# falling edge to DB[7:0] driven (read cycle)	3	--	3	--	ns
t5	CS# hold time	7	--	7	--	ns
t6	AB[15:0] hold time	7	--	7	--	ns
t7	DB[7:0] hold time from RD# rising edge (write cycle)	5	--	5	--	ns
t8	DB[7:0] hold time from RD# rising edge (read cycle)	2	55	2	55	ns
t9	RD# falling edge to valid Data	--	Note 3	--	Note 3	ns
t10	RD# cycle time	Note 4	--	Note 4	--	ns
t11	RD# pulse active time	5	--	5	--	Ts
t12	RD# pulse inactive time	Note 5	--	Note5	--	ns
t13	AS# setup time	0	--	0	--	ns
t14	AS# hold time	0	--	0	--	ns

Note:

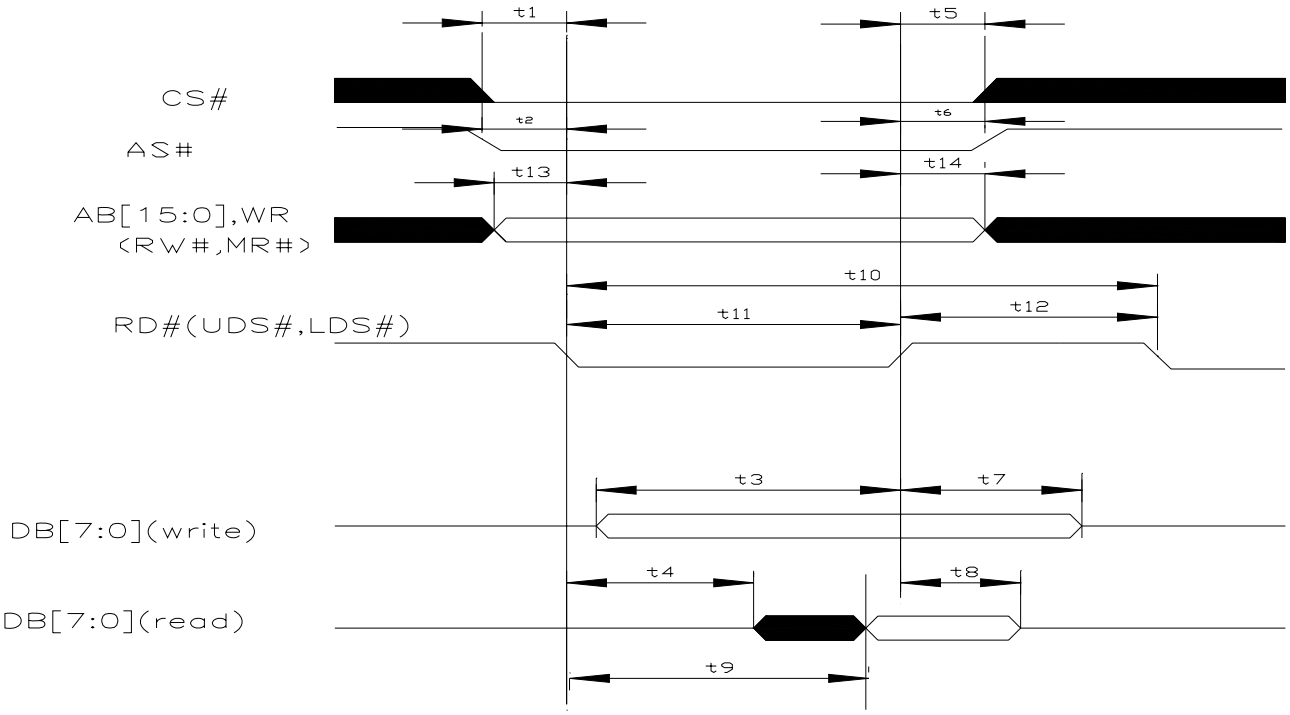
1. Ts = System clock period

2. t3min = 2Ts + 5

3. t9max = 4Ts + 18 (for 3.3V)
= 4Ts + 20 (for 5.0V)

4. t13min = 6Ts (for a read cycle followed by a read or write cycle)
= 7Ts + 2 (for a write cycle followed by a write cycle)
= 10Ts + 2 (for a write cycle followed by a read cycle)

6. t15min = 1Ts (for a read cycle followed by a read or write cycle)
= 2Ts + 2 (for a write cycle followed by a write cycle)
= 5Ts + 2 (for a write cycle followed by a read cycle)



M68K Family Bus Indirect Interface Timing

Note:

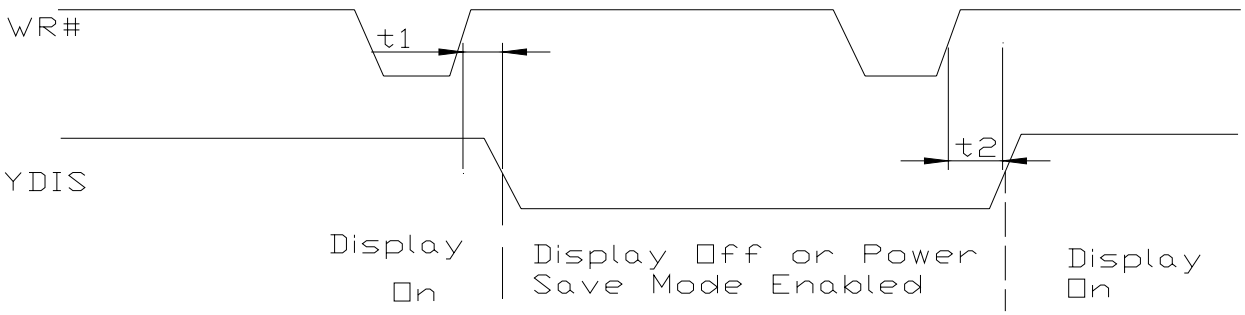
CLK input to the M6800 interface must be driven synchronous to the host microprocessor.

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	--	5	--	ns
t2	AB[15:0] setup time	5	--	5	--	ns
t3	DB[7:0] setup time to RD# falling edge (write cycle)	Note2	--	Note2	--	ns
t4	RD# falling edge to DB[7:0] driven (read cycle)	3	--	3	--	ns
t5	CS# hold time	7	--	7	--	ns
t6	AB[15:0] hold time	7	--	7	--	ns
t7	DB[7:0] hold time from RD# falling edge (write cycle)	5	--	5	--	ns
t8	DB[7:0] hold time from RD# falling edge (read cycle)	2	55	2	55	ns
t9	RD# falling edge to valid Data	--	Note 3	--	Note 3	ns
t10	RD# cycle time	Note 4	--	Note 4	--	ns
t11	RD# pulse active time	5	--	5	--	Ts
t12	RD# pulse inactive time	Note 5	--	Note5	--	ns
t13	AS# setup time	0	--	0	--	ns
t14	AS# hold time	0	--	0	--	ns

Note:

1. Ts = System clock period
2. t3min = 2Ts + 5
3. t9max = 4Ts + 18 (for 3.3V)
   = 4Ts + 20 (for 5.0V)
4. t13min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
6. t15min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

Power Save Mode/Display Enable Timing



Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1a	YDIS falling edge delay for Power Save Mode Enable in Indirect Mode (see Note 2)	--	2	--	2	Frames
t1b	YDIS falling edge delay for Display Off in Indirect Mode (58h)	--	1Ts+10	--	1Ts+10	ns
t1c	YDIS falling edge delay for Display Off in Direct Mode (see Note 3)	--	2Ts+10	--	2Ts+10	ns
t2	YDIS rising edge delay for Display On (see Note 3)	--	2Ts+10	--	2Ts+10	ns

Note:

1. Ts = System Clock Period
2. Power Save Mode is controlled by the Power Save Mode Enable bit, REG[08h] bit 0.
3. Display On/Off is controlled by the Display Enable bit, REG[09h] bit 0.

14. INDIRECT ADDRESSING COMMAND

Indirect Addressing Command

Class	Register Address	Command	Register Description	Control Byte Value	No. of Bytes
System Control	8000h - 8007h	SYSTEM SET	Initializes device and display	40h	8
	8008h	POWER SAVE	Enters standby mode	53h	0
Display Control	8009h - 800A	DISP ON/OFF	Enables/disables display and display attributes	58h 59h	1
	800Bh - 8014h	SCROLL	Sets screen block start addresses and sizes	44h	10
	8015h - 8016h	CSRFORM	Sets cursor type	5Dh	2
	8017h	CSRDIR	Sets direction of cursor movement	4Ch - 4Fh	0
	8018h	OVLAY	Sets display overlay format	5Bh	1
	8019h - 801Ah	CGRAM ADR	Sets start address of character generator RAM	5Ch	2
	801Bh	HDOT SCR	Sets horizontal scroll position	5A	1
Drawing Control	801Ch - 801Dh	CSRW	Sets cursor address	46h	2
	801Eh - 801Fh	CSRR	Reads cursor address	47h	2
	8020h	GRAYSCALE	Sets the Grayscale depth (bpp)	60h	1
Memory Control		MEMWRITE	Writes to memory	42h	n/a
		MEMREAD	Reads from memory	43h	

Command Set

- In general, the internal registers of the SED13700 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged.
- 2-byte parameter (where two bytes are treated as 1 data item) are handled as follows:
  1. CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.
  2. System Set, Scroll, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.
- APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

15. DISPLAY CONTROL FUNCTIONS

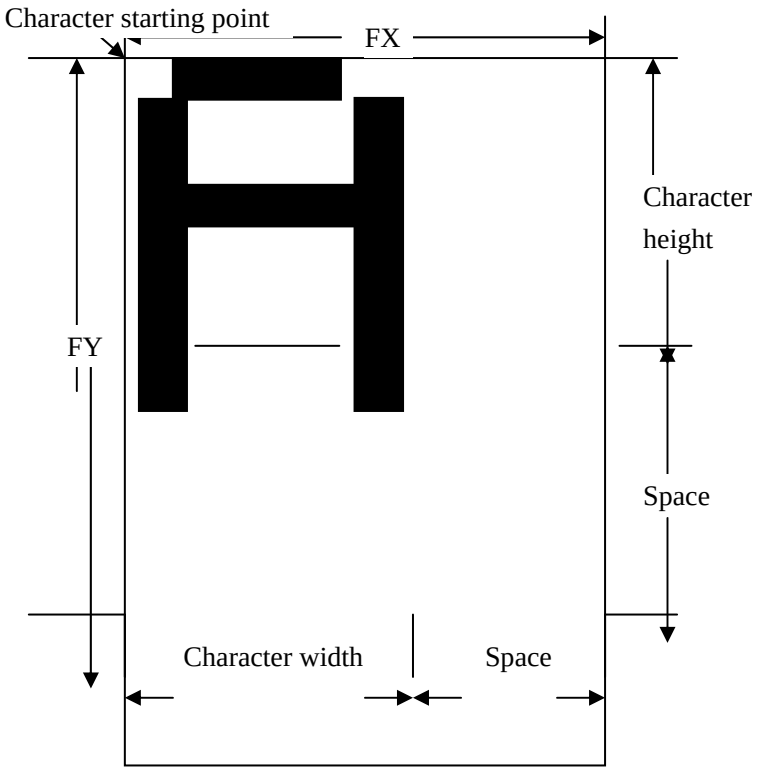
Character Configuration

The origin of each character bitmap is the top left corner. Adjacent bits in each byte are horizontally adjacent in the corresponding character image. Although the size of the bitmap is fixed by the character generator, the actual displayed size of the character field can be varied in both dimensions.

	D7			to				D0
R0	0	1	1	1	0	0	0	0
R1	1	0	0	0	1	0	0	0
R2	1	0	0	0	1	0	0	0
R3	1	0	0	0	1	0	0	0
R4	1	1	1	1	1	0	0	0
R5	1	0	0	0	1	0	0	0
R6	1	0	0	0	1	0	0	0
R7	0	0	0	0	0	0	0	0
R8	0	0	0	0	0	0	0	0
R9	0	0	0	0	0	0	0	0
R10	0	0	0	0	0	0	0	0
R11	0	0	0	0	0	0	0	0
R12	0	0	0	0	0	0	0	0
R13	0	0	0	0	0	0	0	0
R14	0	0	0	0	0	0	0	0
R15	0	0	0	0	0	0	0	0

Space data

Space data



Where:

FX = horizontal character size is 16 pixels (REG[01h] bits 3-0)

FY = vertical character size is 16 pixels (REG[02h] bits 3-0)

16. CHARACTER GENERATOR

16.1. Character Codes

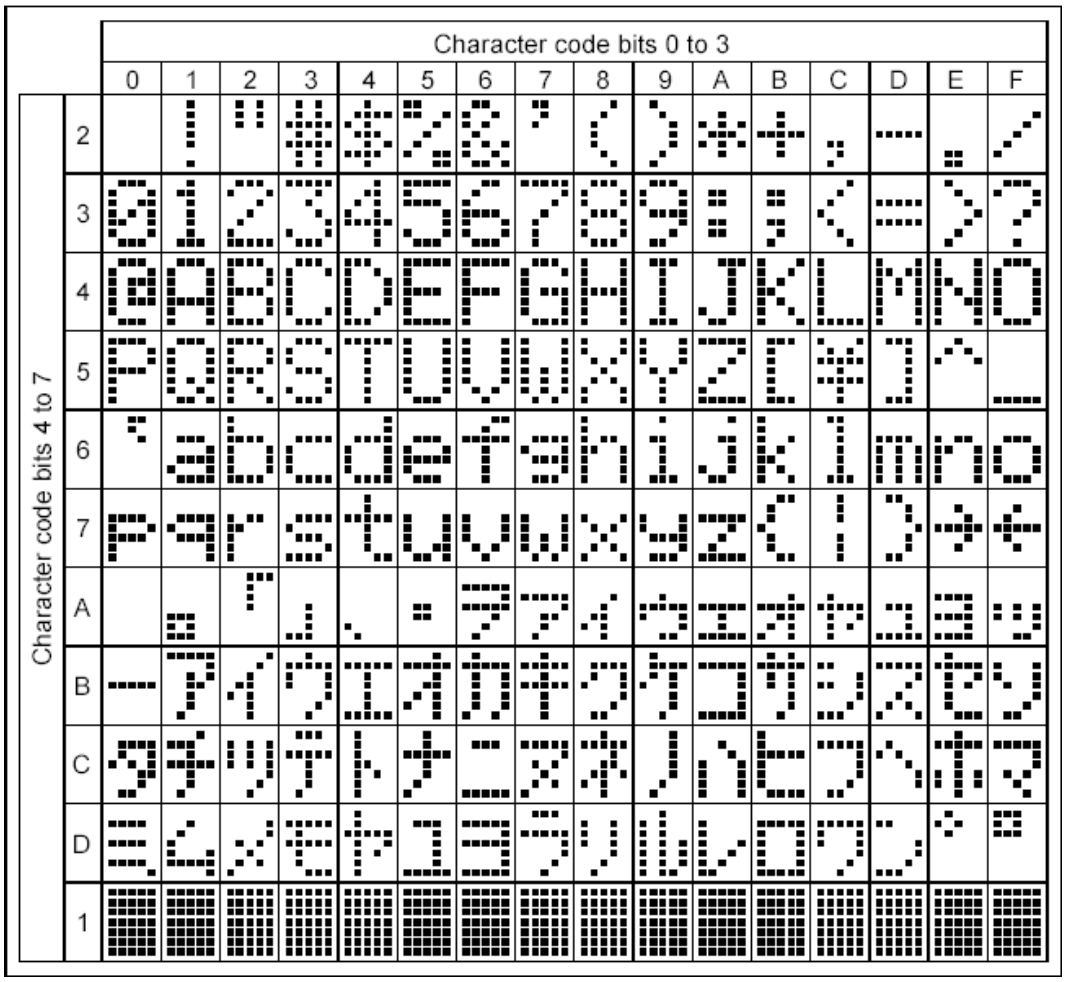
The following figure shows the character codes and the codes allocated to CG RAM. ALL codes can be used by the CG RAM if not using the internal ROM, but the CGRAM address must be set to 0.

Lower 4 bits	Upper 4 bits 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		■		0	@	P	'	p				ー	タ	三		
1		■	!	1	A	Q	a	q			。	ア	チ	ム		
2		■	"	2	B	R	b	r			「	イ	ツ	メ		
3		■	#	3	C	S	c	s			」	ウ	テ	モ		
4		■	$	4	D	T	d	t			、	エ	ト	ヤ		
5		■	%	5	E	U	e	u			・	オ	ナ	ユ		
6		■	&	6	F	V	f	v			ヲ	カ	ニ	ヨ		
7		■	'	7	G	W	g	w			ァ	キ	ヌ	ラ		
8		■	(	8	H	X	h	x			ィ	ク	ネ	リ		
9		■	)	9	I	Y	i	y			ゥ	ケ	ノ	ル		
A		■	*	:	J	Z	j	z			ェ	コ	ハ	レ		
B		■	+	;	K	[	k	{			ォ	サ	ヒ	ロ		
C		■	,	<	L	¥	l	¦			ャ	シ	フ	ワ		
D		■	.	=	M	]	m	}			ュ	ス	ヘ	ン		
E		■	-	>	N	^	n	→			ョ	セ	ホ	゛		
F		■	/	?	O	_	o	←			ッ	ソ	マ	°		

CGRAM1 CGRAM2

On- chip character codes

16.2. Internal Character Generator Font



Note: The shaded positions indicate characters that have the whole 6 · 8 bitmap blackened.

17. MICROPRCESSOR INTERFACE

17.1 .System Bus Interface

CNF[4:0], A[15:1], A0, D[7:0], RD#, WR#, AS and CS are used as control signals for the microprocessor data bus. A0 is normally connected to the lowest bit of the system address bus. CNF[4:2] change the operation of the RD# and WR# pins to enable interfacing to either a Generic (Z80), M6800, or MC68K family bus, and should be pulled-up or pulled-down

Generic

The following table shows the signal states for each function.

Generic Interface Signals

A0	RD#	WR#	Function
1	0	1	Display data and cursor address read
0	1	0	Display data and parameter write
1	1	0	Command write

17.2. M6800 Series

M6800 Series interface signals

A0	R/W#	E	Function
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write
1	0	1	Command write

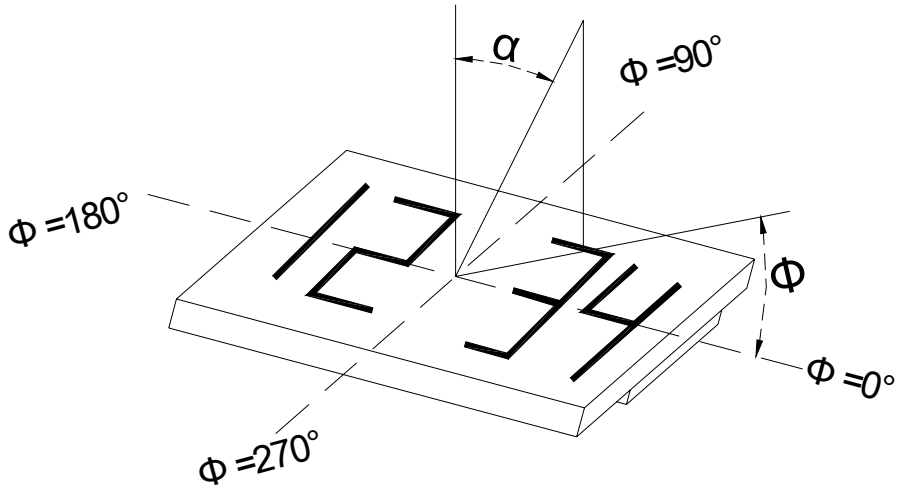
18. OPTICAL CHARACTERISTICS

18.1 Overall optical performance

Positive display

ITEM	SYMBOL	CONDITIONS	TYP.	UNIT	REMARKS
Viewing angles for Contrast Ratio CR > 3	α	Φ = 0° Φ = 90° Φ = 180° Φ = 270°	50 40 50 45	°	Transmissive operation

Definition of viewing angles Φ,α and contrast ratio □R

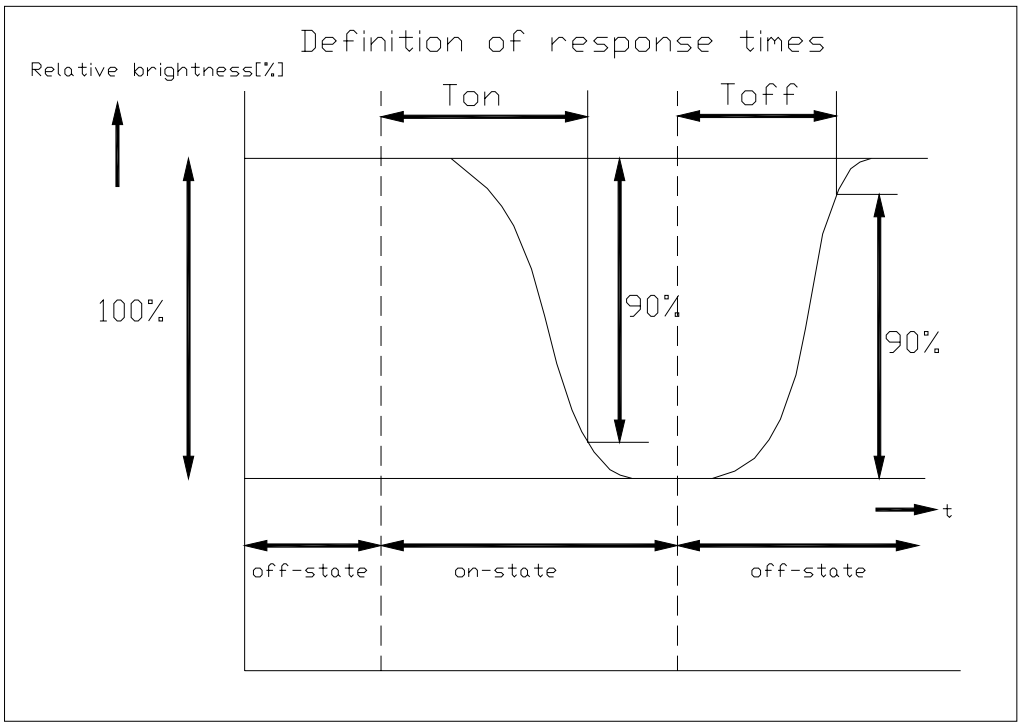


Contrast ratio □R = Brightness of □FF-segmebts / Brightness of □N-segmebts

18.2 Response times at different temperatures

Response times t_{on} and t_{off} are measured using simulated MUX at $f=f_{FRAME}$. Vop (+25°C) will be identical to Vop (+25°C) as specified for the viewing angles.

Item	Symbol	Conditions	Typ.	Max.	Unit	Remarks
Response Times	t_{on}	T_{amb}= +25°C	103.36		ms	α =0°, Φ = 0°
		0°C	371.078		ms	
		-20°C	207.969		ms	
	t_{off}	T_{amb}= +25°C	408.263		ms	
		0°C	1073.424		ms	
		-20°C	4109.318		ms	



19. LCD MODULES HANDLING PRECAUTIONS

- Please remove the protection foil of polarizer before using.

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.

- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.

- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C).Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

20. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.

- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
  - Exposed area of the printed circuit board
  - Terminal electrode sections.